UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,287	01/23/2002	Burnell G. West	M-12401 US	9790

7590 07/29/2004

Deborah Winocur
4057 Amaranta Avenue
Palo Alto, CA 94306

EXAMINER	
LE, JOHN H	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,287	WEST, BURNELL G.	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/09/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/09/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/04/2004 has been entered.

Response to Amendment

2. This office action is in response to applicant's response received on 06/09/2004.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claim 1, line 7, "a resolution of less than one clock cycle" was not described in the specification.

Claim 10, line 2, "a resolution of less than one clock cycle" was not described in the specification.

Claim 20, line 2, line 9, "a resolution of less than one clock cycle" was not described in the specification.

Claim 26, line 2, "a resolution of less than one clock cycle" was not described in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USP 5,642,478) in view of Hoare et al. (US 2002/0133325).

Regarding claims 1 and 10, Chen et al. teach a circuit for time stamping events, the circuit comprising: node controller 38, which read on an event stream distributor coupled to receive the primary event stream (38 receiving 44, Fig.1); and a plurality of timestamp circuits (Col.8, lines 6-13, Col.11, lines 43-45, lines 53-55), each timestamp circuit coupled to receive a respective secondary event stream from the event stream distributor (38 distributing second event, Fig.1).

Chen et al. fail to teach a resolution of less than one clock cycle.

Hoare et al. teach a resolution of less than one clock cycle (a very fast clock cycle that has ten to one-hundred times more resolution than the fastest event)(e.g. [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a resolution of less than one clock cycle as taught by Hoare et al. in a distributed trace data acquisition system of Chen et al. for the purpose of providing new methods and means to compute outcomes many hundreds of times faster than the prior art (Hoare et al., [0031]).

6. Claims 1-5 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelmann et al. (USP 4,894,823) in view of Hoare et al. (US 2002/0133325).

Regarding claims 1 and 10, Adelmann et al. teach a circuit for time stamping events, the circuit comprising: a digital line interface unit 117, which read on an event stream distributor coupled to receive signal from a receive access module 116, which read on the primary event stream (117 receiving 116, Fig.1); and a plurality of timestamp circuits (Col.2, lines 5-26, Col.6, lines 3-8), each timestamp circuit coupled to receive a respective secondary event stream 118 from the event stream distributor 117 (117 distributing second event 118, Fig.1).

Regarding claims 2 and 11, Adelmann et al. teach an event rate in each of the secondary event streams is lower than an event rate in the primary event stream (Col.5, lines 62-67).

Regarding claims 3 and 12, Adelmann et al. teach the relative timing of the events in the primary event stream is maintained in each of the secondary event streams (Col.2, lines 5-26, Col.6, lines 3-8).

Regarding claims 4 and 13, Adelmann et al. teach the primary event stream is a differential signal (116-1 through 116-X, Col.5, lines 51-61).

Regarding claims 5 and 14, Adelmann et al. teach the secondary event streams are differential signals (118-1 through 118-x, Col.5, lines 62-67).

Adelmann et al. fail to teach a resolution of less than one clock cycle.

Hoare et al. teach a resolution of less than one clock cycle (a very fast clock cycle that has ten to one-hundred times more resolution than the fastest event)(e.g. [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of time stamping an event with a resolution of less than one clock cycle as taught by Hoare et al. in a time stamping for packet system of Adelmann et al. for the purpose of providing new methods and means to compute outcomes many hundreds of times faster than the prior art (Hoare et al., [0031]).

7. Claims 26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fransson (USP 5,940,467) in view of Hoare et al. (US 2002/0133325).

Regarding claims 26-29, Fransson teaches a counting circuit, the circuit comprising: a first counter 31 coupled to receive the signal (Fig.1); and a first plurality of gates 71, 72, 73, 74, 75, 76, each gate of the first plurality of gates coupled to receive the signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter 31 (Fig.2, Fig.5A), wherein the first plurality of gates are AND gates, wherein the signal is a differential signal, wherein the signal is a single-ended signal (Col.4, lines 39-65, Col.7, lines 32-67).

Regarding claim 30, Fransson teaches the counter is a Johnson counter (Col.2, lines 5-7).

Regarding claim 31, Fransson teaches the counter is an N-bit counter (Col.2, lines 5-7, Col.4, lines 14-19, Col.5, lines 43-45).

Regarding claim 32, Fransson teaches a second counter 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the second counter (Fig.8, Col.12, lines 45-65).

Fransson fails to teach a resolution of less than one clock cycle.

Hoare et al. teach a resolution of less than one clock cycle (a very fast clock cycle that has ten to one-hundred times more resolution than the fastest event)(e.g. [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of time stamping an event with a resolution of less than one clock cycle as taught by Hoare et al. in a counting circuit of Fransson for the purpose of providing new methods and means to compute outcomes many hundreds of times faster than the prior art (Hoare et al., [0031]).

8. Claims 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boerker (US 2003/0035502 A1) in view of Hoare et al. (US 2002/0133325).

Regarding claim 20, Boerker teaches a data reception circuit for receiving a serial input data stream with a high data transfer rate, the method comprising: receiving the primary event stream 1; a data stream separation circuit 4 distributing rising edge events in the primary event stream among a first plurality of secondary event streams ([0057]); a asynchronously clocked register array 8 recording an arrival time of each event in the first plurality of secondary event streams with respect to a reference clock

([0058]); the data stream separation circuit 4 distributing falling edge events in the primary event stream among a second plurality of secondary event streams ([0057]); and recording an arrival time of each event in the second plurality of secondary event streams with respect to the reference clock ([0058]).

Regarding claim 21, Boerker teaches an event rate in each secondary event stream of the first plurality and the second plurality of secondary event streams is lower than an event rate in the primary event stream ([0057]).

Regarding claim 22, Boerker teaches the primary event stream is a differential signal ([0055]).

Regarding claim 23, Boerker teaches each secondary event stream of the first plurality and the second plurality of secondary event streams are differential signals ([0055]).

Regarding claim 24, Boerker teaches distributing rising edge events comprises selectively enabling a first plurality of gates and distributing falling edge events comprises selectively enabling a second plurality of gates ([0066]).

Regarding claim 25, Boerker teaches distributing rising edge events comprises selectively enabling a first plurality of gates using a first counter 8 that is clocked by the primary event stream and distributing falling edge events comprises selectively enabling a second plurality of gates using a second counter 17 that is clocked by the primary event stream ([0067]).

Boerker fails to teach time stamping an event with a resolution of less than one clock cycle.

Hoare et al. teach a resolution of less than one clock cycle (a very fast clock cycle that has ten to one-hundred times more resolution than the fastest event)(e.g. [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a resolution of less than one clock cycle as taught by Hoare et al. in a data reception circuit of Boerker for the purpose of providing new methods and means to compute outcomes many hundreds of times faster than the prior art (Hoare et al., [0031]).

9. Claims 6-9, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelmann et al. (USP 4,894,823) in view of Hoare et al. (US 2002/0133325) as applied to claims 1 and 10 above, and further in view of Boerker (US 2003/0035502 A1).

Regarding claims 6 and 7, Adelmann et al. and Hoare et al. fail to teach distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

Boerker teaches distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so

on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer ([0056], [0060], [0066], Fig.1, Fig.2).

Regarding claim 8, Boerker teaches distributing rising edge events in the primary event stream among a first plurality of secondary event streams; and distributing falling edge events in the primary event stream among a second plurality of secondary event streams ([0057]).

Regarding claims 9 and 19, Boerker teaches registering the events in each of the secondary event streams ([0055]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream as taught by Boerker in a time stamping for packet system nodes of Adelmann et al. in view of Hoare et al. for the purpose of providing an increasing transfer rate, data or information is transferred via a transfer channel in shorter and shorter times (Boerker, [0005]).

10. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelmann et al. (USP 4,894,823) in view of in view of Hoare et al. (US 2002/0133325) as applied to claim10 above, and further in view of Fransson (USP 5,940,467).

Regarding claims 15-18, Adelmann et al. and Daum et al. fail to teach a first counter coupled to receive the primary event stream; and a first plurality of gates coupled to the first counter, wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter, a second counter coupled to receive the primary event

stream; and a second plurality of gates coupled to the second counter, a plurality of registers, each register operable to register events of one or more secondary event streams.

Fransson teaches a first counter 31 coupled to receive the primary event stream; and a first plurality of gates 71, 72, 73, 74, 75, 76 coupled to the first counter (Fig.1, Fig.2, Fig.3A), wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter (Col.2, lines 5-7), second counters 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4 coupled to the second counter, each register operable to register events of one or more secondary event streams (Fig.8, Col.12, lines 45-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a counter, plurality of gates coupled to the counter, wherein the counter is a Johnson counter, wherein the counter is an N-bit counter as taught by Fransson in a time stamping for packet system nodes of Adelmann et al. in view of Hoare et al. for the purpose of providing a counting circuit, the resolution of which is equal to the cycle time of the first clock signal applied to the counting circuit (Fransson, Col.2, lines 46-48).

Response to Arguments

11. Applicant's arguments filed 06/04/2004 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach "time stamping an event with a resolution of less than one clock cycle".

"Timestamping events in each of secondary event stream with a resolution of less than one clock cycle" was not described in the specification.

In paragraph 5 that related art: "a timestamp circuit is a circuit that is responsive to a reference clock and that creates a digital representation of the time at which an event occurs. The digital representation of the time at which an event occurs has two components. The first component is the specific clock cycle of the reference clock within which the event occurs. The second component is the time at which the event occurs within the specific clock cycle of the reference clock. Since each event is represented by the two components which are generated with respect to a reference clock, subsequent processing steps can easily determine timing relationships between each event which is useful when debugging/testing an integrated circuit device".

The paragraph 5 is unclear to describe "timestamping events in each of secondary event stream with a resolution of less than one clock cycle".

Hoare et al. teach a resolution of less than one clock cycle (a very fast clock cycle that has ten to one-hundred times more resolution than the fastest event)(e.g. [0017]).

Conclusion

12. Specifically Hoare et al. has been added to another ground of rejection.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

July 14, 2004

John Barlow
Supervisory Patent Examiner
Technology Center 2800